PACKAGED, CASCADABLE WIDEBAND MONOLITHIC FEEDBACK AMPLIFIERS FOR RADAR SYSTEMS APPLICATIONS

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ABSTRACT

Design criteria and fabrication of a packaged, monolithic, cascadable, feedback amplifier are presented. The good performances in term of bandwidth, gain, flatness, reproducibility and reliability makes this component highly suitable for many radar applications.

INTRODUCTION

Modern radar systems contain a large number of receive and transmit channels which utilise general purpose amplifiers (medium power and noise level), with low input/output VSWR. For such applications the intrinsic advantages of the GaAs microwave monolithic integrated circuit (MMIC) technology can be employed to obtain extremely uniform performance, low cost integrated circuits for use in compact integrated electronics sub-systems, designed to minimize the overall dimensions of the RF section.

In this article we will outline the fabrication steps of high-reliability, packaged, cascadable wideband monolithic amplifiers for radar systems operating up to 6 Ghz.

CIRCUIT MODEL

Generally, amplifier design for radar systems applications needs components with good performances in term of stability, bandwidth, flatness, low group delay and good phase linearity. The design of a constant-gain amplifier over a wide frequency range mainly concerns the design of the matching network in order to compensate for the $|S21|$ variations with frequency and matching of the input and output port over a wide range of frequency. Among the various design methods [1] we used the negative feedback method which seems to be more advantageous for our application.

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MESFET DIMENSIONING

From the theory of feedback amplifiers [2], the well known relationships, $Rfb = gm\ Zo^2$ and $G = 20\ Log\ (gm\ Zo - 1)$, allow easy dimensioning of the matched stage at low frequencies. In our case, at the upper frequency limit, it is impossible to neglect the effects of the reactive elements. So a trade-off between the transconductance and the input and output capacitances is needed. For this reason we have preferred a low noise technology, which minimises the gm/C ratio. A MESFET with a 0.5x600 um gate which gives an input capacitance of 0.6 pF and a transconductance of 70 mS at Vg=0, has been chosen. This device is suitable for integration in monolithic feedback amplifiers having our requirements.

FEEDBACK AMPLIFIER DESIGN

The MESFET "S" parameters have been measured at different d.c. bias voltages, using the TRL deembedding method.
To eliminate interconnection effects, the equivalent circuit has been obtained with numerical fitting methods. This equivalent circuit has been used in a single stage feedback network optimisation in order to obtain a flat gain amplifier up to 6 Ghz. This preliminary layout has been optimised to take into account geometrical discontinuities, by means of an electromagnetic simulator (LINMIC +).

The yield has been carefully maximised. In fact the number of components, the areas of capacitors and the overall dimension of the circuit have been reduced.

The optimised values of the circuit element have been centred in the technological range in order to maximise the electrical yield with statistical methods (Montecarlo analysis).

In fig. 1a and b we can see the amplifiers schematic circuits. The three-stages amplifier have been designed for a 20 dB gain, whilst the two-stages amplifiers have been designed to have 10 dB gain. Moreover, in order to increase the yield, the amplifier in fig. 1b, has a bias configuration which eliminates the d.c. block capacitors both in the feedback and interstage network.

FABRICATION

Standard processing techniques are used for amplifier fabrication. MESFET'isolation was achieved by selective ion-implantation of the donor species (N_{Si}=1E13 at 40 kev plus 5E12 at 120 kev). The 0.5x600 um interdigitated gate was realised by conventional hard contact lithography using positive resist. A reactively sputtered Si_3N_4 layer (3000 A

thick) was used as the capacitor dielectric material. All other process steps used conventional metallizations, passivation lift-off and gold-plating techniques. The thickness of GaAs substrate is 220 um and the dimensions of the 3-stage and 2-stage amplifiers (shown in Figg. 2 and 3) are 2.45x1.65 and 1.45x1.65 mm respectively.

APPLICATION AND PACKAGING

Apart from systems with a large variety of components (such as phased array radars), the number of amplifiers in a radar system is usually quite small. When the use of an amplifier as a "building block" in several subassemblies and in different radar systems is possible, the amount of components increases reaching a number that makes monolithic technology suitable for this task. In this application, wideband, easy to integrate, small size and highly reproducible and reliable MMIC's are required.

The above considerations have led to the choice of a packaged component, which to fulfil the 10 to 40 dB gain requirements can contain up to two monolithic chips in an hermetically sealed housing. The main characteristics that a package must have, are the hermetic sealing, a low thermal resistance and an easy integrability in supercomponents.

The chosen package has been submitted to a thorough RF characterisation. In order to evaluate the electrical discontinuity of a single feed-through, deembedding methods in the time and frequency domains have been used. Fig.4.

The obtained results guarantee the proper performance in the interested frequency range.

Fig. 5 shows a packaged monolithic chip photograph.

EXPERIMENTAL RESULTS

Fig 6 a and b show the packaged monolithic amplifiers experimental results. The gain-ripple is found to be better than +/- 0.25 dB over a 10% bandwidth, +/- 0.5 dB over a 25 % bandwidth and +/-1.5 dB for the overall 2 to 6 Ghz band. The input and output return loss are typically 15 dB and always better than 10 dB. Noise figure is better than 4 dB and 1 dB compression point is about + 20 dBm. The thermal resistance of the packaged chip is found to be 70 C/W, assuring safe operation even with environmental temperature of 70 C according to the MIL requirements.

A considerable number of amplifiers passed the following tests:

- stabilisation bake: 48 hours at case temperature + 100 °C.
- Temperature cycling: 5 cycles from -30 °C to +80 °C with no noticeable degradation of performance when re-tested.

CONCLUSION

This paper describes the benefits that can be obtained from a correctly applied monolithic integrated circuit technology in terms of performances and costs. By extending the design procedure to other radars components it is foreseen that in near future the radar systems engineers will have at their disposal whole range of packaged MMIC components with field-tested reliability.

References

[1] R.SOARES,"GaAs MESEFET Circuit Design," Artech House Inc.

[2] K.B.NICLAS et al.,"The Matched Feedback Amplifier: Ultrawide Band Microwave Amplification With GaAs MESFET's," IEEE Trans. Microwave Theory Tech. Vol. MTT-28, pp 285-294, Apr. 1980.

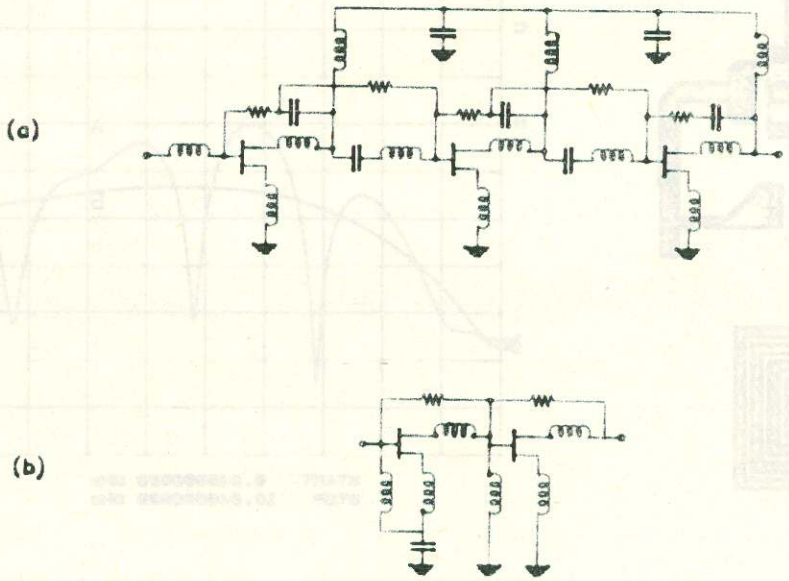

Fig. 1. Schematic Circuit of feedback amplifiers
(a) three-stage. (b) two-stage

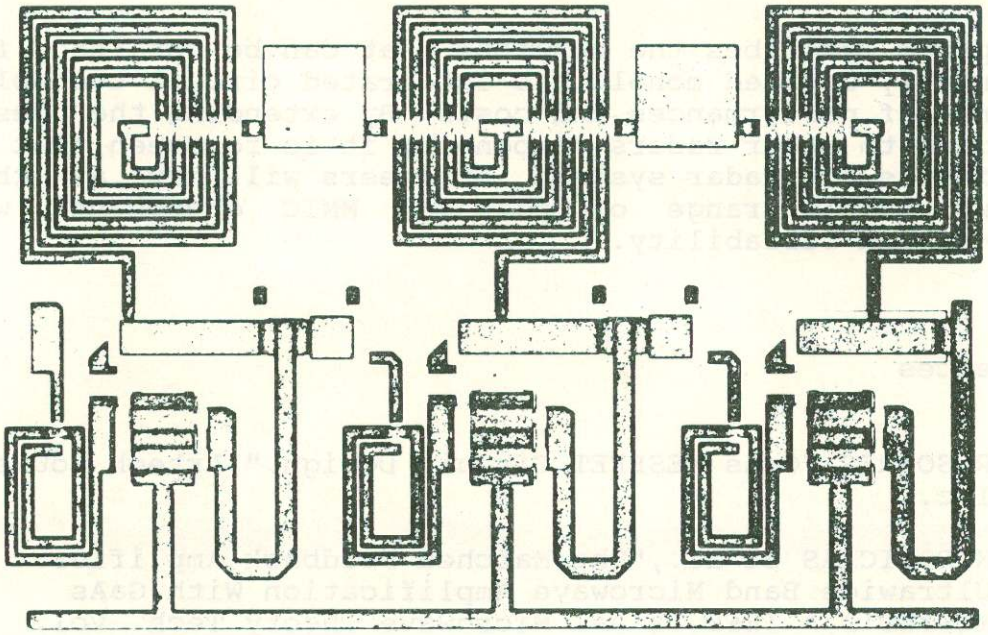

Fig. 2 Monolithic three-stage amplifier

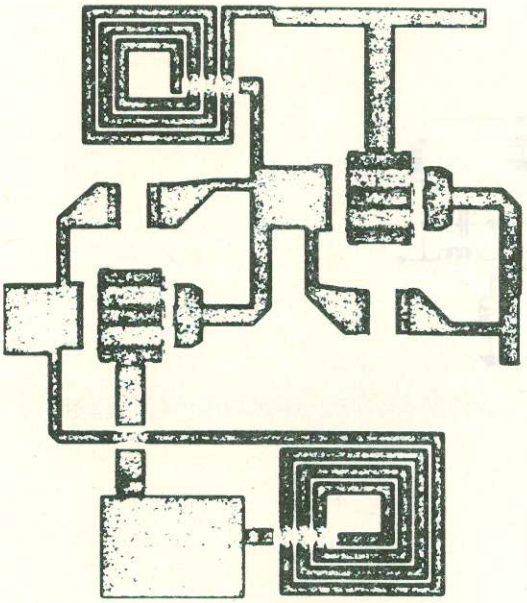

Fig. 3 Monolithic two-stage amplifier

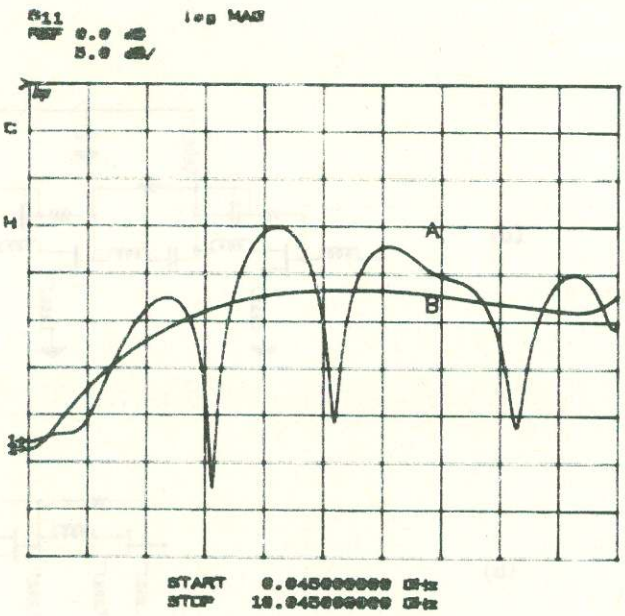

Fig. 4 Package performance
A) Overall return loss
B) Single RF terminal return loss

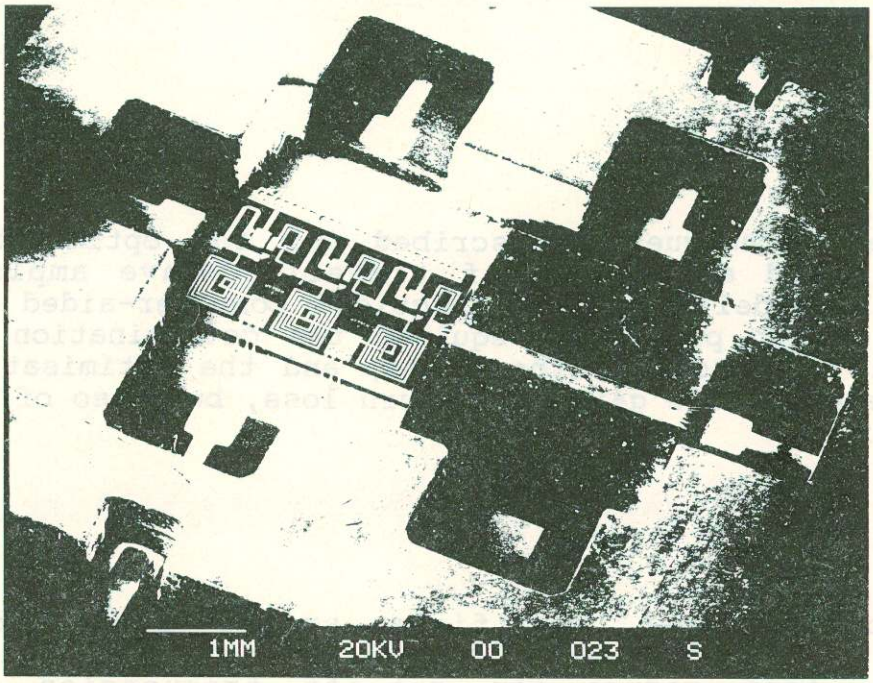

Fig. 5 Packaged monolithic chip

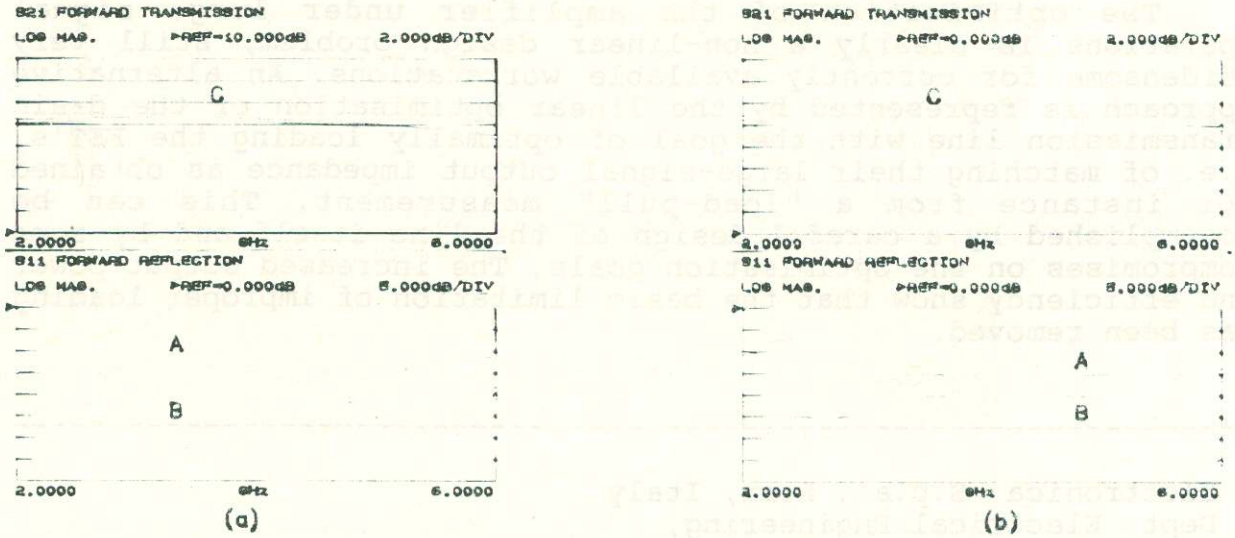

Fig. 6 Electrical performances. Trace A) S11 . Trace B) S22 . Trace C) S21
(a) Three-stage amplifier (B) two-stage amplifier